

Atty. Docket No. CPAC 1017-5
Appl. No. 10/632,552

PATENT

OFFICE

Amendments to the Specification

JAN 10 2005

Please replace paragraph [0022] with the following amended paragraph:

The top BGA in this configuration is similar to the bottom BGA, except that the top BGA has z-interconnect solder balls 338 connected (through solder vias 335 in the top substrate) to the metal layer 331 a metal layer 331 only at the periphery of the top substrate. Solder balls 338 are reflowed onto the metal layer 31 of the bottom substrate to provide the z-interconnect. Particularly, the top BGA in this configuration includes a substrate 332 having ~~a patterned metal layer 331~~ the patterned metal layer 331 onto which the top BGA die 334 is connected by flip chip bumps 336. Between the top BGA die and substrate is a polymer underfill 333. A structure as in FIG. 3 is more appropriate for high electrical performance applications, but it has similar limitations to configurations of the type shown in of FIG. 2. It presents an improvement over the FIG. 2 configuration in that the bottom BGA has no molding, allowing for use of smaller diameter (h) solder balls at the periphery of the top BGA for connection between the packages.

Please replace paragraph [0068] with the following amended paragraph:

In the top LGA package in the embodiment of FIG. 5A the die is wire bonded onto wire bond sites on the upper metal layer of the substrate to establish electrical connections. The die 514 and the wire bonds 516 are encapsulated with a molding compound 517 that provides protection from ambient and from mechanical stress to facilitate handling operations, and has a top package upper surface 519. The top package 500 is stacked over the bottom package 400 and affixed there using an adhesive ~~[[513]]~~ 503. Solder masks 515, 527 are patterned over the metal layers 521, 523 to expose the underlying metal at bonding sites for electrical connection, for example the wire bond sites for bonding the wire bonds 516.

Please replace paragraph [0096] with the following amended paragraph:

Alternatively, the top heat spreader can be a generally planar piece of a thermally conductive material such as, for example, a sheet of metal (such as copper), with no supporting members. At least the more central area of the upper surface of the planar heat spreader is exposed to ambient for efficient heat exchange away from the MPM. Such a simple planar heat spreader is shown in FIG. 6D at 1004, where the heat spreader is affixed to an upper surface of the top package molding. The construction of the stacked packages in MPM ~~[[1004]]~~ 107 is generally

Atty. Docket No. CPAC 1017-5
Appl. No. 10/632,552

PATENT

similar to that of MPM 1044 109 in FIG. 6E, and like structures are identified in the FIGS. by like reference numerals. The top heat spreader 1004 in the example of FIG. 6D is a generally planar piece of a thermally conductive material having at least the more central area of its upper surface exposed to ambient for efficient heat exchange away from the MPM, as in the example of FIG. 6E. The top heat spreader may be, for example, a sheet of metal (such as copper). Here, however, the top heat spreader 1004 is affixed onto the upper surface 1019 of the upper package encapsulant 1017 using an adhesive 1006. The adhesive 1006 may be a thermally conductive adhesive, to provide improved heat dissipation. Usually the top heat spreader is affixed to the top package molding after the top package molding has been at least partly cured, but before the molding material is injected for the MPM encapsulation 1007. The periphery of the top heat spreader may be encapsulated with the MPM molding material. In the embodiment of FIG. 6D a step like re-entrant feature 1005 is provided on the periphery of the heat spreader 1004 to allow for better mechanical integrity of the structure with less delamination from the molding compound.

Please replace paragraph [0100] with the following amended paragraph:

[[FIG. 17]] FIG. 7 is a flow diagram showing a process for assembly of a multi-package module as shown for example in FIG. 6A or FIG. 6B. In a step 1702, an unsingulated strip of die-up flip chip ball grid array packages is provided. The flip chip interconnects are protected by an underfill or molding between the die and the die attach surface of the bottom substrate, and so no overmolding is required. The BGA packages in the strip preferably are tested (as indicated in the FIG. by *) for performance and reliability before they are taken to subsequent steps in the process. Only packages identified as "good" are subjected to subsequent treatment. In a step 1704, adhesive is dispensed over the upper surface of the substrate on "good" BGA packages. In a step 1706, singulated second packages are provided, which may be stacked die packages, as for example in FIGS. 6A and 6B. The singulated second packages are protected by a molding, and preferably are tested (*) and identified as "good". In a step 1708, a pick-and-place operation is carried out to place "good" second packages on the adhesive over the substrate on the "good" BGA packages. In a step 1710, the adhesive is cured. In a step 1712, a plasma clean operation is performed in preparation for a step 1714 in which wire bond z-interconnections are formed between the stacked top (stacked die) and bottom die-up flip chip BGA packages. In a step 1716, an additional plasma clean may be performed, followed by the formation of the MPM molding in a step 1718. In a step 1720, the second-level interconnect solder balls are attached to the underside of the module. In a

Atty. Docket No. CPAC 1017-5
Appl. No. 10/632,552

PATENT

step 1722, the completed modules are tested (*) and singulated from the strip, for example by saw singulation or by punch singulation, and packaged for further use.